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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,720	09/08/2003	David R. Czajkowski		8237

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EXAMINER
LOHN, JOSHUA A

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,720	CZAJKOWSKI ET AL.	
	Examiner	Art Unit	
	Joshua A. Lohn	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Statutory Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 12 and 13 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 7 and 8 of copending Application No. 10/435,626. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claims 12 and 13 directed to the same invention as that of claims 7 and 8 of commonly assigned copending Application No. 10/435,626. The issue of priority under 35 U.S.C. 102(g) and possibly 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP Chapter 2300), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

Non-Statutory Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 6-11 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 of copending Application No. 10/435,626 in view of Hosaka et al., United States Patent number 4,956,807, published September 11, 1990, in view of Davis, United States Patent number 5,345,583, published September 6, 1994, in further view of Baylocq, United States Patent number 5,822,515, published October 13, 1998.

The copending application discloses, in copending claims 1-6 all the limitations of claims 6-11, except for those involving the hardened core circuit, timer signal resets, and timer initiated interrupts and resets.

Hosaka discloses a microprocessor (Hosaka, col. 2, line 41); an array of memory, volatile or non-volatile, connected to said microprocessor (Hosaka, col. 2, lines 41-43); a core circuit

connected to said microprocessor (Hosaka, col. 2, lines 40-45, where the watchdog timer is the core circuit), in a manner allowing for connection to the data bus and address bus signals (Hosaka, col. 2, lines 41-43, where the bus is well known to include address and data bus information, col. 2, lines 29-30), and interrupt control, reset control, interrupt output, and power cycle output signal (Hosaka, col. 4, lines 54-61). Hosaka further discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the said hardened core circuit on a predetermined time period (Hosaka, col. 2, lines 55-58); and the core circuit configured to read predetermined timer signal from said microprocessor on predetermined time period and activate said microprocessor's interrupt and reset control input signals if timer signal is not received within predetermined time period to provide for removal of said microprocessor from functionally interrupted state (Hosaka, col. 3, lines 14-30 and col. 2, lines 55-58, where the functionally interrupted state is the abnormal status).

It would have been obvious to one skilled in the art at the time the invention was made to include the watchdog timer of Hosaka in the invention of Czajkowski.

This would have been obvious because Czajkowski discloses a desire to have an embodiment featuring a watchdog circuit without providing full details of its operation (Czajkowski, ¶19). Hosaka provides these operational details to fill the obvious need of Czajkowski (Hosaka, col. 1, lines 51-55). Czajkowski and Hosaka fail to disclose the core circuit being hardened. Hosaka and Czajkowski further fail to disclose a microprocessor software routine configured to restart the application software.

Davis discloses a microprocessor software routine located at said microprocessor's interrupt or reset vector addresses, configured to restart the microprocessor's application software

(Davis, col. 4, lines 14-25).

It would have been obvious to one skilled in the art at the time of the invention to include the extra reset controls in the watchdog timer environment of Czajkowski and Hosaka.

This would have been obvious because Hosaka discloses a desire to maintain a system executing in a normal state (Hosaka, col. 3, lines 25-27). Davis also discloses a desire to maintain execution in the normal state through the use of timers (Davis, col. 4, lines 40-45). Davis provides the additional improvement of providing a system that maintains critical data across reset boundaries to improve upon the time required to restore operation (Davis, col. 3, lines 5-18). This improved restoration time would obviously have furthered Hosaka's desire to reduce the amount of time the system spent in abnormal functional states. The combination of Czajkowski, Hosaka and Davis still fails to disclose that the core circuit is hardened.

Baylocq discloses hardening a watchdog circuit and CPU (Baylocq, col. 3, lines 40-42).

It would have been obvious to one skilled in the art at the time of the invention to use the hardening of Baylocq on the watchdog circuit of Czajkowski, Hosaka and Davis.

This would have been obvious because Hosaka discloses a desire to allow the watchdog circuit to function in an environment that is susceptible to strong charges and noise (Hosaka, col. 5, lines 1-5), and Baylocq discloses that the hardening will allow the functioning of a system in environments of strong charges (Baylocq, col. 2, lines 10-15). It would have been obvious at the time to shield the invention of Czajkowski, Hosaka and Davis using the hardening of Baylocq to further these goals.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 recites the limitation "the VLIW microprocessor" in line 7. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination it will be assumed that the microprocessor of claims 6-10 is a VLIW microprocessor.

Claim Objections

Claims 6, 11, and 8 are objected to because of the following informalities:

In claim 6, line 7, it states "identical and spatially separated". Based upon the context and the structure of other claims the examiner interprets it as being equivalent to "identical and being inserted into spatially separated", for purposes of examination.

In claim 11, line 3, it states "a very long instruction word microprocessor", in order to clarify the language that is later used the examiner recommends changing the language to "a very long instruction word (VLIW) microprocessor".

In claim 11, line 10, to avoid a rejection based upon indefinite claim language, "with a VLIW" should be changed to "with the VLIW".

In claim 11, line 12, "a third inserted" should be changed to "a third instruction inserted", it will be interpreted as such for purposes of examination.

In claim 11, line 13, "computational units" should be changed to "computational unit".

In claim 13, line 7, "time interval is the first" should be changed to "time interval if the first", and will be interpreted as such for the purposes of examination.

Appropriate correction of each objection is required.

Applicant is advised that should claim 6 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Jitsukawa et al., United States Patent number 4,670,880, published June 2, 1987.

As per claim 12, Jitsukawa discloses a method of processing data in a fault tolerant computer system, comprising: generating a first instruction at a first time interval; generating a second instruction identical to the first instruction at a second time interval; generating a third instruction identical to the first and second instructions at a third time interval (Jitsukawa, col. 2, line 57, through col. 3, line 15, where the three instructions are identical when generated, and before being transformed, and return to this original state for comparison, col. 3, lines 23-39); comparing the first, second and third instructions (Jitsukawa, col. 3, lines 40-45); matching anyone of the first, second, or third instructions to each other (Jitsukawa, col. 3, lines 40-45); and performing an action based on the match instruction (Jitsukawa, col. 2, lines 45-56).

Claims 12 and 13 rejected under 35 U.S.C. 102(e) as being anticipated by Czajkowski, United States Patent Application Publication number 2004/0153747, filed May 6, 2003.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 12, Czajkowski discloses a method of processing data in a fault tolerant computer system, comprising: generating a first instruction at a first time interval; generating a second instruction identical to the first instruction at a second time interval; generating a third instruction identical to the first and second instructions at a third time interval; comparing the first, second and third instructions; matching anyone of the first, second, or third instructions to each other; and performing an action based on the match instruction (Czajkowski, ¶7).

As per claim 13, Czajkowski discloses a method of processing data in a fault tolerant computer system, comprising: generating a first instruction at a first time interval; generating a second instruction identical to the first instruction at a second time interval; comparing the first and second instructions to each other; performing an action based on the matched first and second instructions; generating a third instruction identical to the first and second instructions at a third time interval is the first and second instructions do not match; matching the first, second, and third instructions to each other; and performing an action based on a match between anyone of the first, second, and third instructions (Czajkowski, ¶8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosaka et al., United States Patent number 4,956,807, published September 11, 1990, in view of Davis, United States Patent number 5,345,583, published September 6, 1994, in further view of Baylocq, United States Patent number 5,822,515, published October 13, 1998.

As per claim 1, Hosaka discloses a computer system with improved tolerance to microprocessor functional interrupts induced by environmental sources, comprising: a microprocessor (Hosaka, col. 2, line 41); an array of memory, volatile or non-volatile, connected to said microprocessor (Hosaka, col. 2, lines 41-43); a core circuit connected to said microprocessor (Hosaka, col. 2, lines 40-45, where the watchdog timer is the core circuit), in a manner allowing for connection to the data bus and address bus signals (Hosaka, col. 2, lines 41-43, where the bus is well known to include address and data bus information, col. 2, lines 29-30), and interrupt control, reset control, interrupt output, and power cycle output signal (Hosaka, col. 4, lines 54-61). Hosaka further discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the said hardened core circuit on a predetermined time period (Hosaka, col. 2, lines 55-58); and the core circuit configured to read predetermined timer signal from said microprocessor on predetermined time period and activate said microprocessor's interrupt and reset control input signals if timer signal is not received within predetermined time period to provide for removal of said microprocessor from

functionally interrupted state (Hosaka, col. 3, lines 14-30 and col. 2, lines 55-58, where the functionally interrupted state is the abnormal status). Hosaka fails to disclose the core circuit being hardened. Hosaka further fails to disclose a microprocessor software routine configured to restart the application software.

Davis discloses a microprocessor software routine located at said microprocessor's interrupt or reset vector addresses, configured to restart the microprocessor's application software (Davis, col. 4, lines 14-25).

It would have been obvious to one skilled in the art at the time of the invention to include the extra reset controls in the watchdog timer environment of Hosaka.

This would have been obvious because Hosaka discloses a desire to maintain a system executing in a normal state (Hosaka, col. 3, lines 25-27). Davis also discloses a desire to maintain execution in the normal state through the use of timers (Davis, col. 4, lines 40-45). Davis provides the additional improvement of providing a system that maintains critical data across reset boundaries to improve upon the time required to restore operation (Davis, col. 3, lines 5-18). This improved restoration time would obviously have furthered Hosaka's desire to reduce the amount of time the system spent in abnormal functional states. The combination of Hosaka and Davis still fails to disclose that the core circuit is hardened.

Baylocq discloses hardening a watchdog circuit and CPU (Baylocq, col. 3, lines 40-42).

It would have been obvious to one skilled in the art at the time of the invention to use the hardening of Baylocq on the watchdog circuit of Hosaka and Davis.

This would have been obvious because Hosaka discloses a desire to allow the watchdog circuit to function in an environment that is susceptible to strong charges and noise (Hosaka, col.

5, lines 1-5), and Baylocq discloses that the hardening will allow the functioning of a system in environments of strong charges (Baylocq, col. 2, lines 10-15). It would have been obvious at the time to shield the invention of Hosaka and Davis using the hardening of Baylocq to further these goals.

As per claim 2, Hosaka, Davis, and Baylocq further disclose a system of claim 1 further comprising a microprocessor software routine configured to send maintenance data to microprocessor memory prior to functional interrupt and configured to read said maintenance data from microprocessor memory after microprocessor's removal from functionally interrupted state and use maintenance data to restart microprocessor's application software routines (Davis, col. 4, lines 4-13).

As per claim 3, Hosaka, Davis, and Baylocq further disclose the system of claim 2 further comprising a microprocessor software routine configured to read said hardened core status signal(s), and to determine if interrupt or reset activation was result of hardened core activation and then restart application software routines, or normal interrupt or reset and then continue with normal application software operation (Davis, col. 4, lines 14-25, where the activation signal causes interruption and reset).

As per claim 4, Hosaka, Davis, and Baylocq further disclose the system of claim 3 further comprising a microprocessor software routine configured to halt all currently operating application software threads (Davis, col. 4, lines 14-25, where all operation is ceased).

As per claim 5, Hosaka, Davis, and Baylocq further disclose the system of claim 4 further comprising a microprocessor software routine configured to read hardened core status signal(s), and to determine if multiple functional interrupts occurred within predetermined time period and

then to restart all microprocessor software and hardware if multiple functional interrupts occurred within predetermined time period (Davis, col. 4, lines 34-45, where multiple time signal interrupts cause the full reset), or, if single functional interrupt occurred in predetermined time period to then to read maintenance data stored in said memory and provide a controlled restart of selected application software (Davis, col. 4, lines 14-25, where one timer notification is received to initiate the reading of critical maintenance data).

Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Czajkowski, United States Patent Application Publication number 2004/0153747, filed May 6, 2003, in view of Hosaka et al., United States Patent number 4,956,807, published September 11, 1990, in view of Davis, United States Patent number 5,345,583, published September 6, 1994, in further view of Baylocq, United States Patent number 5,822,515, published October 13, 1998.

As per claim 6, Czajkowski discloses a computer system with improved fault tolerance from microprocessor data errors and functional interrupts, comprising: a microprocessor; a fault tolerant software routine configured to send a first instruction and at least a second instruction to the microprocessor, the first and at least the second instructions being identical and spatially separated functional computational units of the VLIW microprocessor in at different clock cycles; a first and at least a second memory device in communication with the microprocessor, the first memory device configured to store the first instruction, the second memory device configured to store at least the second instruction; a software instruction to compare the first instruction to at least the second instruction; a comparator to compare the first instruction to the

second instruction (Czajkowski, ¶5). Czajkowski fails to disclose a hardened core circuit, timer controls, and associated reset operations.

Hosaka discloses a microprocessor (Hosaka, col. 2, line 41); an array of memory, volatile or non-volatile, connected to said microprocessor (Hosaka, col. 2, lines 41-43); a core circuit connected to said microprocessor (Hosaka, col. 2, lines 40-45, where the watchdog timer is the core circuit), in a manner allowing for connection to the data bus and address bus signals (Hosaka, col. 2, lines 41-43, where the bus is well known to include address and data bus information, col. 2, lines 29-30), and interrupt control, reset control, interrupt output, and power cycle output signal (Hosaka, col. 4, lines 54-61). Hosaka further discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the said hardened core circuit on a predetermined time period (Hosaka, col. 2, lines 55-58); and the core circuit configured to read predetermined timer signal from said microprocessor on predetermined time period and activate said microprocessor's interrupt and reset control input signals if timer signal is not received within predetermined time period to provide for removal of said microprocessor from functionally interrupted state (Hosaka, col. 3, lines 14-30 and col. 2, lines 55-58, where the functionally interrupted state is the abnormal status).

It would have been obvious to one skilled in the art at the time the invention was made to include the watchdog timer of Hosaka in the invention of Czajkowski.

This would have been obvious because Czajkowski discloses a desire to have an embodiment featuring a watchdog circuit without providing full details of its operation (Czajkowski, ¶19). Hosaka provides these operational details to fill the obvious need of Czajkowski (Hosaka, col. 1, lines 51-55). Czajkowski and Hosaka fail to disclose the core circuit

being hardened. Hosaka and Czajkowski further fail to disclose a microprocessor software routine configured to restart the application software.

Davis discloses a microprocessor software routine located at said microprocessor's interrupt or reset vector addresses, configured to restart the microprocessor's application software (Davis, col. 4, lines 14-25).

It would have been obvious to one skilled in the art at the time of the invention to include the extra reset controls in the watchdog timer environment of Czajkowski and Hosaka.

This would have been obvious because Hosaka discloses a desire to maintain a system executing in a normal state (Hosaka, col. 3, lines 25-27). Davis also discloses a desire to maintain execution in the normal state through the use of timers (Davis, col. 4, lines 40-45). Davis provides the additional improvement of providing a system that maintains critical data across reset boundaries to improve upon the time required to restore operation (Davis, col. 3, lines 5-18). This improved restoration time would obviously have furthered Hosaka's desire to reduce the amount of time the system spent in abnormal functional states. The combination of Czajkowski, Hosaka and Davis still fails to disclose that the core circuit is hardened.

Baylocq discloses hardening a watchdog circuit and CPU (Baylocq, col. 3, lines 40-42).

It would have been obvious to one skilled in the art at the time of the invention to use the hardening of Baylocq on the watchdog circuit of Czajkowski, Hosaka and Davis.

This would have been obvious because Hosaka discloses a desire to allow the watchdog circuit to function in an environment that is susceptible to strong charges and noise (Hosaka, col. 5, lines 1-5), and Baylocq discloses that the hardening will allow the functioning of a system in environments of strong charges (Baylocq, col. 2, lines 10-15). It would have been obvious at the

time to shield the invention of Czajkowski, Hosaka and Davis using the hardening of Baylocq to further these goals.

As per claim 7, Czajkowski, Hosaka, Davis, and Baylocq disclose the system of claim 6 further comprising a third instruction sent by the fault tolerant software routine to the microprocessor, the third instruction stored in a third memory device in communication with the microprocessor (Czajkowski, ¶15-¶16).

As per claim 8, Czajkowski, Hosaka, Davis, and Baylocq disclose the system of claim 7 wherein the software instruction directs the comparator to compare the first, second, and third instruction (Czajkowski, ¶15-¶16).

As per claim 9, Czajkowski, Hosaka, Davis, and Baylocq disclose the system of claim 8 wherein a match of the any of the first, second, and third instructions is accepted by the microprocessor (Czajkowski, ¶15-¶16).

As per claim 10, Czajkowski, Hosaka, Davis, and Baylocq disclose the system of claim 6 wherein the microprocessor comprises a VLIW microprocessor (Czajkowski, ¶14).

As per claim 11, Czajkowski discloses a software and hardware computer system with improved fault tolerance from microprocessor data errors and functional interrupts, comprising: a very long instruction word microprocessor; an array of memory, volatile or non-volatile, connected to said microprocessor; a fault tolerant software routine comprising a first instruction and a second instruction, each inserted into two spatially separate functional computational units in the VLIW microprocessor at two different clock cycles and stored in a memory device in communication with the microprocessor, the first and second instructions being identical; a

software instruction to compare the first and second instruction in the memory device in communication with a VLIW microprocessor compare or branch units, and configured to perform an action if the first and second instruction match, the fault tolerant software routine comprising a third inserted into a third spatially separate functional computational units in the VLIW microprocessor at a third different clock cycles and stored in a third memory device in communication with the microprocessor, the first, second, and third instructions being identical; the software instruction to compare the first, second, and third instructions in the memory devices in communication with a VLIW microprocessor compare or branch units, and configured to perform an action if any of the first, second and third instructions match (Czajkowski, ¶6). Czajkowski fails to disclose a hardened core circuit, timer controls, and associated reset operations.

Hosaka discloses a microprocessor (Hosaka, col. 2, line 41); an array of memory, volatile or non-volatile, connected to said microprocessor (Hosaka, col. 2, lines 41-43); a core circuit connected to said microprocessor (Hosaka, col. 2, lines 40-45, where the watchdog timer is the core circuit), in a manner allowing for connection to the data bus and address bus signals (Hosaka, col. 2, lines 41-43, where the bus is well known to include address and data bus information, col. 2, lines 29-30), and interrupt control, reset control, interrupt output, and power cycle output signal (Hosaka, col. 4, lines 54-61). Hosaka further discloses a microprocessor software routine configured to send a predetermined timer signal from the microprocessor to the said hardened core circuit on a predetermined time period (Hosaka, col. 2, lines 55-58); and the core circuit configured to read predetermined timer signal from said microprocessor on predetermined time period and activate said microprocessor's interrupt and reset control input

signals if timer signal is not received within predetermined time period to provide for removal of said microprocessor from functionally interrupted state (Hosaka, col. 3, lines 14-30 and col. 2, lines 55-58, where the functionally interrupted state is the abnormal status).

It would have been obvious to one skilled in the art at the time the invention was made to include the watchdog timer of Hosaka in the invention of Czajkowski.

This would have been obvious because Czajkowski discloses a desire to have an embodiment featuring a watchdog circuit without providing full details of its operation (Czajkowski, ¶19). Hosaka provides these operational details to fill the obvious need of Czajkowski (Hosaka, col. 1, lines 51-55). Czajkowski and Hosaka fail to disclose the core circuit being hardened. Hosaka and Czajkowski further fail to disclose a microprocessor software routine configured to restart the application software.

Davis discloses a microprocessor software routine located at said microprocessor's interrupt or reset vector addresses, configured to restart the microprocessor's application software (Davis, col. 4, lines 14-25).

It would have been obvious to one skilled in the art at the time of the invention to include the extra reset controls in the watchdog timer environment of Czajkowski and Hosaka.

This would have been obvious because Hosaka discloses a desire to maintain a system executing in a normal state (Hosaka, col. 3, lines 25-27). Davis also discloses a desire to maintain execution in the normal state through the use of timers (Davis, col. 4, lines 40-45). Davis provides the additional improvement of providing a system that maintains critical data across reset boundaries to improve upon the time required to restore operation (Davis, col. 3, lines 5-18). This improved restoration time would obviously have furthered Hosaka's desire to

reduce the amount of time the system spent in abnormal functional states. The combination of Czajkowski, Hosaka and Davis still fails to disclose that the core circuit is hardened.

Baylocq discloses hardening a watchdog circuit and CPU (Baylocq, col. 3, lines 40-42).

It would have been obvious to one skilled in the art at the time of the invention to use the hardening of Baylocq on the watchdog circuit of Czajkowski, Hosaka and Davis.

This would have been obvious because Hosaka discloses a desire to allow the watchdog circuit to function in an environment that is susceptible to strong charges and noise (Hosaka, col. 5, lines 1-5), and Baylocq discloses that the hardening will allow the functioning of a system in environments of strong charges (Baylocq, col. 2, lines 10-15). It would have been obvious at the time to shield the invention of Czajkowski, Hosaka and Davis using the hardening of Baylocq to further these goals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A. Lohn whose telephone number is (571) 272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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